WHAT IS CLAIMED IS:

1. A semiconductor device having a plurality of wiring layers in a multi-layered structure,

said semiconductor device including an inner area at a surface and a pad area surrounding said inner area therein,

said semiconductor device comprising a device fabricated below said pad area.

2. The semiconductor device as set forth in claim 1, wherein said device is comprised of at least one of a bypass capacitor, a protection device, and an input/output device.

3. The semiconductor device as set forth in claim 1, further comprising a second device fabricated below said device,

said device being comprised of a bypass capacitor,

said second device being comprised of at least one of a protection device and an input/output device.

4. The semiconductor device as set forth in claim 2, wherein said bypass capacitor is comprised of metal wire layers arranged below said pad area.

5. The semiconductor device as set forth in claim 4, wherein each of said metal wire layers is comprised of a first wire and a second wire with an interlayer insulating layer being sandwiched therebetween,

said first wire being electrically connected to a voltage source,

said second wire being grounded.

6. The semiconductor device as set forth in claim 4, wherein each of said

metal wire layers is comprised of a first comb-shaped wire being electrically connected to a voltage source and a second comb-shaped wire being grounded,

said first and second wires being arranged such that teeth of said first comb-shaped wire are located between teeth of said second comb-shaped wire in the same plane.

7. The semiconductor device as set forth in claim 5, further comprising at least one of first to fourth pads in said pad area,

said first pad being electrically connected to said input/output device,

said second pad being electrically connected to said first wire,

said third pad being electrically connected to said second wire,

said fourth pad being not electrically connected to said input/output device, said first wire and said second wire.

8. A semiconductor device having a plurality of wiring layers in a multi-layered structure,

said semiconductor device including an inner area at a surface, an input/output area surrounding said inner area therein, and a pad area surrounding said input/output area therein,

said semiconductor device including a plurality of input/output terminals in said input/output area, and a plurality of pads in said pad area,

said semiconductor device including (a) a first source voltage wire being electrically connected to a voltage source and surrounding said inner area in said pad area, and (b) a first ground wire being grounded and surrounding said first source voltage wire in said pad area,

each of said pads being electrically connected to any one of said input/output terminals, said first source voltage wire, and said first ground wire,

said first source voltage wire being comprised of a plurality of first metal wiring layers in a multi-layered structure, said first metal wiring layers being

electrically connected to one another through via-holes formed through first interlayer insulating films sandwiched between said first metal wiring layers,

said first ground wire being comprised of a plurality of second metal wiring layers in a multi-layered structure, said second metal wiring layers being electrically connected to one another through via-holes formed through said first interlayer insulating films,

each of said first metal wiring layers and each of said second metal wiring layers being formed in the same layer,

vertically adjacent first and second metal wiring layers with one of said first interlayer insulating films being sandwiched therebetween, among said first and second metal wiring layers, defining a bypass capacitor.

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~~8~~. The semiconductor device as set forth in claim ~~8~~, further comprising:

(c) a second source voltage wire being electrically connected to a voltage source and surrounding said inner area in said input/output area, and

(d) a second ground wire being grounded and surrounding said second source voltage wire in said input/output area,

said second source voltage wire being comprised of a plurality of third metal wiring layers in a multi-layered structure, said third metal wiring layers being electrically connected to one another through via-holes formed through second interlayer insulating films sandwiched between said third metal wiring layers,

said second ground wire being comprised of a plurality of fourth metal wiring layers in a multi-layered structure, said fourth metal wiring layers being electrically connected to one another through via-holes formed through said second interlayer insulating films,

each of said third metal wiring layers and each of said fourth metal wiring layers being formed in the same layer,

vertically adjacent third and fourth metal wiring layers with one of said second interlayer insulating films being sandwiched therebetween, among said

third and fourth metal wiring layers, defining a bypass capacitor.

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10. The semiconductor device as set forth in claim 9, wherein said first source voltage wire is electrically connected to said second source voltage wire, and said first ground wire is electrically connected to said second ground wire.

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11. The semiconductor device as set forth in claim 9, wherein said first source voltage wire is comprised of a first comb-shaped wire being electrically connected to a voltage source, and said first ground wire is comprised of a second comb-shaped wire being grounded,

said second source voltage wire is comprised of a third comb-shaped wire being electrically connected to a voltage source, and said second ground wire is comprised of a fourth comb-shaped wire being grounded,

said first and second wires being arranged such that teeth of said first comb-shaped wire are located between teeth of said second comb-shaped wire in the same plane,

said third and fourth wires being arranged such that teeth of said third comb-shaped wire are located between teeth of said fourth comb-shaped wire in the same plane.

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12. The semiconductor device as set forth in claim 11, wherein said first source voltage wire is electrically connected to said second source voltage wire, and said first ground wire is electrically connected to said second ground wire.

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13. The semiconductor device as set forth in claim 8, further comprising a protection device fabricated below said bypass capacitor,

said protection device comprising:

(a) a substrate formed at a surface with a first well having a first electrical conductivity and a second well having a second electrical conductivity;

(b) a first interlayer insulating film formed on said substrate;

(c) a first layer formed on said first interlayer insulating film;

(d) a second interlayer insulating film formed on said first layer; and

(e) a signal wiring layer formed on said second interlayer insulating film,

said first layer including one of said first metal wiring layers, one of said second metal wiring layers, and a second signal wiring layer all electrically connected to said first or second well through via-holes formed through said first interlayer insulating film,

said second signal wiring layer being electrically connected to said signal wiring layer through via-holes formed through said second interlayer insulating film.

14. The semiconductor device as set forth in claim 8, wherein said input/output area has an extended portion located below said pad area,

said extended portion comprising:

(a) a substrate formed at a surface with a first well having a first electrical conductivity and a second well having a second electrical conductivity;

(b) a first interlayer insulating film formed on said substrate;

(c) a first layer formed on said first interlayer insulating film;

(d) a second interlayer insulating film formed on said first layer; and

(e) a signal wiring layer formed on second interlayer insulating film,

said first layer including one of said first metal wiring layers electrically connected to said first well through a via-hole formed through said first interlayer insulating film, one of said second metal wiring layers electrically connected to said second well through a via-hole formed through said first interlayer insulating film, and a second signal wiring layer electrically connected to said first or second well through via-holes formed through said first interlayer insulating film,

said second signal wiring layer being electrically connected to said signal

wiring layer through via-holes formed through said second interlayer insulating film.

15. A semiconductor device having a plurality of wiring layers in a multi-layered structure,

said semiconductor device including an inner area at a surface, an input/output area surrounding said inner area therein, and a pad area surrounding said input/output area therein,

said semiconductor device including a plurality of input/output terminals in said input/output area, and a plurality of pads in said pad area,

said semiconductor device including (a) a first source voltage wire being electrically connected to a voltage source and surrounding said inner area in said pad area, and (b) a first ground wire being grounded and surrounding said first source voltage wire in said pad area,

each of said pads being electrically connected to any one of said input/output terminals, said first source voltage wire, and said first ground wire,

said semiconductor device including a protection device fabricated below said pad area,

said protection device comprising:

(a) a substrate formed at a surface with a first well having a first electrical conductivity and a second well having a second electrical conductivity;

(b) a first interlayer insulating film formed on said substrate;

(c) a first layer formed on said first interlayer insulating film;

(d) a second interlayer insulating film formed on said first layer; and

(e) a signal wiring layer formed on second interlayer insulating film,

said first layer including one of said first metal wiring layers, one of said second metal wiring layers, and a second signal wiring layer all electrically connected to said first or second well through via-holes formed through said first interlayer insulating film,

said second signal wiring layer being electrically connected to said signal wiring layer through via-holes formed through said second interlayer insulating film.

16. A semiconductor device having a plurality of wiring layers in a multi-layered structure,

said semiconductor device including an inner area at a surface, an input/output area surrounding said inner area therein, and a pad area surrounding said input/output area therein,

said semiconductor device including a plurality of input/output terminals in said input/output area, and a plurality of pads in said pad area,

said semiconductor device including (a) a first source voltage wire being electrically connected to a voltage source and surrounding said inner area in said pad area, and (b) a first ground wire being grounded and surrounding said first source voltage wire in said pad area,

each of said pads being electrically connected to any one of said input/output terminals, said first source voltage wire, and said first ground wire,

said input/output area having an extended portion located below said pad area,

said extended portion comprising:

(a) a substrate formed at a surface with a first well having a first electrical conductivity and a second well having a second electrical conductivity;

(b) a first interlayer insulating film formed on said substrate;

(c) a first layer formed on said first interlayer insulating film;

(d) a second interlayer insulating film formed on said first layer; and

(e) a signal wiring layer formed on second interlayer insulating film,

said first layer including one of said first metal wiring layers electrically connected to said first well through a via-hole formed through said first interlayer insulating film, one of said second metal wiring layers electrically connected to

said second well through a via-hole formed through said first interlayer insulating film, and a second signal wiring layer electrically connected to said first or second well through via-holes formed through said first interlayer insulating film,

said second signal wiring layer being electrically connected to said signal wiring layer through via-holes formed through said second interlayer insulating film.

17. A method of fabricating a semiconductor device having a plurality of wiring layers in a multi-layered structure, and having an inner area at a surface and a pad area surrounding said inner area therein,

said method comprising the steps of:

(a) forming said inner area; and

(b) fabricating a device below said pad area,

said steps (a) and (b) being to be concurrently carried out.

18. The method as set forth in claim 17, wherein at least one of a bypass capacitor, a protection device, and an input/output device is fabricated as said device in said step (b).

19. The method as set forth in claim 17, further comprising the step of (c) fabricating a second device below said device.

20. The method as set forth in claim 19, wherein said step (c) is carried out concurrently with said steps (a) and (b).

21. The method as set forth in claim 19, wherein a bypass capacitor is fabricated as said device in said step (b), and at least one of a protection device and an input/output device is fabricated as said second device in said step (c).